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09/927,204	08/10/2001	Martin Foltin	10011094-1	3853

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EXAMINER	
STEVENS, THOMAS H	
ART UNIT	**PAPER NUMBER**
2123	

DATE MAILED: 11/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/927,204	FOLTIN ET AL.	
	Examiner	Art Unit	
	Thomas H. Stevens	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 August 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/10/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 were examined.

Claim Interpretation

2. Office personnel are to give claims their **"broadest reasonable interpretation"** in light of the supporting disclosure. *In re Morris,* 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027-28 (Fed. Cir. 1997). Limitations appearing in the specification but not recited in the claim are not read into the claim. *In re Prater,* 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-551(CCPA 1969). See *also *In re Zletz,* 893 F.2d 319, 321-22, 13 USPQ2d 1320, 1322(Fed. Cir. 1989) ("During patent examination the pending claims must be interpreted as broadly as their terms reasonably allow") .... The reason is simply that during patent prosecution when claims can be amended, ambiguities should be recognized, scope and breadth of language explored, and clarification imposed .... An essential purpose of patent examination is to fashion claims that are precise, clear, correct, and unambiguous. Only in this way can uncertainties of claim scope be removed, as much as possible, during the administrative process. The examiner declares the claim feature of the clock signal active after each data input passes each latch as a design choice for the reason being that whether the signal arrives before or after the time interval relative to the clock is immaterial since the circuit may not function in either case.

Claim Rejections - 35 USC § 103

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-20 are rejected under 35 U.S.C. 103 (a) as unpatentable by Rizzolo (U.S. Patent 6,453,436 (2000)), in view of Segal (U.S. Patent 6,023,568 (2000)) and in further view Avidan (U.S. Patent 6,158,022 (2000)).

Rizzolo teaches a method to scan a series of latch circuitry (abstract) with the subsequent function of using "dummy" latches to propagate a transition of integrated circuits; but doesn't teach a methodology of sequence timing nor transparent elements or their delays. Segal teaches a method and an apparatus for constructing a model of a

digital circuit, which contains level sensitive latches while Avidan, teaches a circuit analyzer for black, gray and transparent elements (title).

At the time the invention, it would have been obvious to one of ordinary skill in the art to use Avidan and Segal to modify Rizzolo since it would be advantageous to have the ability to design various time scenarios for any applicable integrated circuit simulation application.

Claim 1. A method for verifying a minimal level sensitive timing abstraction model, comprising (Segal: column 7, lines 4-25 and column 8, lines 18-36): extracting a plurality of parameters from a modeled circuit that includes sequential elements controlled by clock elements (Avidan: column 2, lines 60-67); creating an echo-circuit that represents the plurality of parameters with nodes and time arcs (Rizzolo: column 6, lines 23-26); wherein the echo-circuit is lightweight and can be input into any static timing analysis (STA) tools (Segal: column 7, lines 4-25), and wherein the echo-circuit enables a signal to propagate from an input port to an output port only if the signal arrives at the output port later than a clock signal from a most critical clock element controlling the output port (design choice: see claim interpretation); identifying relevant timing paths in the echo-circuit, wherein the relevant timing paths are associated with the plurality of parameters (Segal: column 7, lines 4-25 and column 8, lines 18-36); identifying paths in the modeled circuit (Segal: column 9, lines 64-67) that connect sequential elements and correspond to the relevant timing paths in the echo-circuit; and

comparing the relevant timing paths in the echo-circuit with the corresponding paths in the modeled circuit (Segal: columns 9 and 10, lines 49-67 and 1-6).

Claim 2. The method of claim 1, (Segal: column 7, lines 4-25 and column 8, lines 18-36; Rizzolo: column 6, lines 23-26; Avidan: column 2, lines 60-67) wherein the extracting the plurality of parameters step includes extracting a required time parameter (Avidan: column 5, lines 20-21) associated with a setup check node.

Claim 3. The method of claim 1, (Segal: column 7, lines 4-25 and column 8, lines 18-36; Rizzolo: column 6, lines 23-26; Avidan: column 2, lines 60-67) wherein the extracting the plurality of parameters step includes extracting a required time parameter associated with a hold check node (Avidan: column 1, lines 60-65).

Claim 4. The method of claim 1; (Segal: column 7, lines 4-25 and column 8, lines 18-36; Rizzolo: column 6, lines 23-26; Avidan: column 2, lines 60-67) wherein the extracting the plurality of parameters step includes extracting a valid time parameter associated with a dummy latch node (Rizzolo: column 12, lines 39-42), wherein the dummy latch node is controlled by the most critical clock element (Segal: column 9, lines 27-37).

Clam 5. The method of claim 1, (Segal: column 7, lines 4-25 and column 8, lines 18-36; Rizzolo: column 6, lines 23-26; Avidan: column 2, lines 60-67) wherein the extracting the plurality of parameters step includes extracting a transparent delay arc parameter

(Avidan: column 18, lines27-31 and 57-61) that represents a time delay a signal passes from an input port to an output port of the modeled circuit.

Claim 6.The method of claim 1, (Segal: column 7, lines 4-25 and column 8, lines 18-36; Rizzolo: column 6, lines 23-26; Avidan: column 2, lines 60-67) further comprising modifying names of the nodes in the echo-circuit to correspond to names (Avidan: column 5, lines 29-33) of corresponding sequential elements in the modeled circuit.

Claim 7. The method of claim 1, (Segal: column 7, lines 4-25 and column 8, lines 18-36; Rizzolo: column 6, lines 23-26; Avidan: column 2, lines 60-67) further comprising generating an error report if the relevant timing paths (Avidan: column 12, lines 55-60) in the echo-circuit do not match the corresponding paths in the modeled circuit.

Claim 8. The method of claim 1, (Segal: column 7, lines 4-25 and column 8, lines 18-36; Rizzolo: column 6, lines 23-26; Avidan: column 2, lines 60-67) wherein the creating the echo-circuit step includes creating a timing abstraction model that is port-based (Avidan: column 6, lines 13-23).

Claim 9. The method of claim 1, (Segal: column 7, lines 4-25 and column 8, lines 18-36; Rizzolo: column 6, lines 23-26; Avidan: column 2, lines 60-67) wherein the creating the echo-circuit step includes creating a timing abstraction model that has level triggered

latches (Avidan: column 2, lines 31-33. Note: applicant equivocates level triggered latches and transparent latches; specification, pg. 3, lines 32-33).

Claim 10. The method of claim I, (Segal: column 7, lines 4-25 and column 8, lines 18-36; Rizzolo: column 6, lines 23-26; Avidan: column 2, lines 60-67) wherein the creating the echo-circuit step includes creating a timing abstraction models that is stimulus independent (Avidan: column 6, lines 41-42).

Claim 11. An apparatus for verifying a minimal level sensitive timing abstraction model, comprising (Segal: column 7, lines 4-25 and column 8, lines 18-36): means for extracting a plurality of parameters from a modeled circuit that includes sequential elements (Avidan: column 2, lines 60-67) controlled by clock elements; means for creating an echo-circuit that represents the plurality of parameters with nodes and time arcs (Rizzolo: column 6, lines 23-26), wherein the echo-circuit is lightweight and can be input into any static timing analysis (STA) tools (Segal: column 7, lines 4-25), and wherein the echo-circuit enables a signal to propagate from an input port to an output port only if the signal arrives at the output port later than a clock signal from a most critical clock element controlling the output port (design choice: see claim interpretation); means for identifying relevant timing paths in the echo-circuit, wherein the relevant timing paths are associated with the plurality of parameters (Segal: column 7, lines 4-25 and column 8, lines 18-36); means for identifying paths in the modeled circuit that connect sequential elements and correspond to the relevant timing paths in

the echo-circuit; and means for comparing the relevant timing paths in the echo-circuit with the corresponding paths in the modeled circuit (Avidan: column 3, lines 19-26).

Claim 12. The apparatus of claim 11, (Segal: column 7, lines 4-25 and column 8, lines 18-36; Avidan: column 2, lines 60-67; Rizzolo: column 6, lines 23-26) further comprising means for modifying names (Avidan: column 5, lines 29-33) of the nodes in the echo-circuit to correspond to names of corresponding sequential elements in the modeled circuit.

Claims 13. The apparatus of claim 11, (Segal: column 7, lines 4-25 and column 8, lines 18-36; Avidan: column 2, lines 60-67; Rizzolo: column 6, lines 23-26) further comprising means for generating an error report if the relevant timing paths in the echo-circuit do not match the corresponding paths in the modeled circuit (Avidan: column 12, lines 55-60).

Claims 14. A computer readable medium providing instructions for verifying a minimal level sensitive timing abstraction model, (Segal: column 7, lines 4-25 and column 8, lines 18-36) the instructions comprising: extracting a plurality of parameters from a modeled circuit (Avidan: column 2, lines 60-67) that includes sequential elements controlled by clock elements creating an echo-circuit that represents the plurality of parameters with nodes and time arcs, (Rizzolo: column 6, lines 23-26) wherein the echo-circuit is lightweight and can be input into any static timing analysis (STA) tools,

(Segal: column 7, lines 4-25) and wherein the echo-circuit enables a signal to propagate from an input port to an output port only if the signal arrives at the output port later than a clock signal from a most critical clock element controlling the output port; identifying relevant timing paths in the echo-circuits wherein the relevant timing paths are associated with the plurality of parameters (Segal: column 9, lines 64-67); identifying paths in the modeled circuit (Segal: column 9, lines 64-67) that connect sequential elements and correspond to the relevant timing paths in the echo-circuit; and comparing the relevant timing paths in the echo-circuit with the corresponding paths in the modeled circuit (Segal: columns 9 and 10, lines 49-67 and 1-6).

Claim15. The computer readable medium of claim 14, (Segal: column 7, lines 4-25 and column 8, lines 18-36; Avidan: column 2, lines 60-67; Rizzolo: column 6, lines 23-26) further comprising instructions for modifying names of the nodes (Avidan: column 5, lines 29-33) in the echo-circuit to correspond to names of corresponding sequential elements in the modeled circuit.

Claim 16. The computer readable medium of claim 14, (Segal: column 7, lines 4-25 and column 8, lines 18-36; Avidan: column 2, lines 60-67; Rizzolo: column 6, lines 23-26) further comprising instructions for generating an error report if the relevant timing paths in the echo-circuit do not match the corresponding paths in the modeled circuit (Avidan: column 12, lines 55-60).

Claim 17. The computer readable medium of claim 14, (Segal: column 7, lines 4-25 and column 8, lines 18-36; Avidan: column 2, lines 60-67; Rizzolo: column 6, lines 23-26) wherein the instructions for extracting the plurality of parameters (Avidan: column 5, lines 20-21) step includes for instructions extracting a required time parameter associated with a setup check node.

Claim 18. The computer readable medium of claim 14, (Segal: column 7, lines 4-25 and column 8, lines 18-36; Avidan: column 2, lines 60-67; Rizzolo: column 6, lines 23-26) wherein the instnzctions for extracting the plurality of parameters step includes instructions for extracting a required time parameter associated with a hold check node (Avidan: column 1, lines 60-65).

Claim 19. The computer readable medium of claim 14, (Segal: column 7, lines 4-25 and column 8, lines 18-36; Avidan: column 2, lines 60-67; Rizzolo: column 6, lines 23-26) wherein the instructions for extracting the plurality of parameters step includes instructions for extracting a valid time parameter associated with a dummy latch node (Rizzolo: column 12, lines 39-42).

Claim 20. The computer readable medium of claim 14, (Segal: column 7, lines 4-25 and column 8, lines 18-36; Avidan: column 2, lines 60-67; Rizzolo: column 6, lines 23-26) wherein the instructions for extracting the plurality of parameters step includes instructions for extracting a transparent delay arc parameter (Avidan: column 18, lines

27-31 and 57-61) that represents a time delay a signal passes from an input port to an output port of the modeled circuit.

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mr. Tom Stevens whose telephone number is (571) 271-0365, Monday-Friday (8:00 am- 4:30 pm) or contact Supervisor Mr. Kevin Teska at (571) 272-3716. The fax number for the group is 703-308-1396.

Any inquires of general nature or relating to the status of this application should be directed to the Group receptionist whose phone number is (571)272-1400

October 26, 2004

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